REMARKS

In response to the Office Action mailed April 20, 2004, Applicant respectfully requests reconsideration. To further the prosecution of this Application, Applicant submits the following remarks and has canceled claims. Applicant prays that, after consideration of these remarks, a favorable decision will be provided regarding the claims.

Claims 1-42 were pending in this Application. Claims 30-31 and 41-42 have been canceled without prejudice as to the subject matter recited therein. Applicant expressly reserves the right to prosecute the canceled claims and similar claims in one or more related Applications. Accordingly, claims 1-29 and 32-40 are now pending in this Application. Claims 1, 11 and 21 are independent claims.

Rejection under §103

Claims 1-29 and 32-40 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,425,034 (Steinmetz et al.). Applicant respectfully traverses this rejection and requests reconsideration. The claims are believed to be in allowable condition.

Steinmetz discloses a host system 180 having a host bus adaptor 182 which connects to a number of peripheral devices 186 through a high-speed serial FC data stream 188 (column 8, lines 45-54 and Figs. 4 and 5). The host bus adaptor 182 utilizes a fibre channel controller 190 (column 8, lines 55-58). Steinmetz further discloses a disk array controller 200 which uses the fibre channel controller 190 (column 8, lines 64-65 and Figs. 5 and 6). For example, the disk array controller 200 includes a cache memory 210 which connects to an FC controller 206 through a PCI bus 208, and connects to other FC controllers 216A-216N through another PCI bus 214 to interface to a mass storage system 204 (column 9, lines 1-8 and Fig. 6).

Claims 1-10 and 32-35

Claim 1 is directed to a method for exchanging data with a volatile memory cache circuit. The method is performed in an interface circuit of a data storage system. The method includes the steps of providing a command to the volatile memory cache circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit, moving a data element through the point-to-point channel in accordance with the command, and receiving status from the volatile memory cache circuit through the point-to-point channel in accordance with the data element.

The cited prior art does not teach a method for exchanging data with a volatile memory cache circuit which has a step of providing a command to the volatile memory cache circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit, as recited in claim 1. To the contrary, Steinmetz discloses an FC controller 206 which communicates with a cache memory 210 through a multi-drop PCI bus 208 (e.g., see column 8, lines 49-52; column 9, lines 1-4 and Fig. 6 of Steinmetz).

If one were to attempt to argue that the FC controller 206 of Steinmetz provides a command to the cache memory 210, Steinmetz clearly would not involve providing a command to a volatile memory cache circuit through a point-to-point channel as recited in claim 1. Rather, Steinmetz would involve providing the command to cache memory 210 through the multi-drop PCI bus 208 through which the microprocessor 212 also communicates (e.g., see Fig. 6 of Steinmetz). The mult-drop PCI bus 208 is clearly not a point-to-point channel, but rather is a potential source of significant latency due to the presence of the microprocessor 212. For example, a drawback of this approach is that access to the cache memory 210 is limited due to bus contention as explained in the Specification on page 3, lines 8-17.

Additionally, if one were to attempt to argue that the host system 202 is an interface circuit, Steinmetz clearly does not involve providing a command to a volatile memory cache circuit through a point-to-point channel between the

interface circuit and a volatile memory cache circuit as recited in claim 1. Rather, Steinmetz would involve providing a command to an FC controller 206 through an FC between a host system 202 and the FC controller 206 (e.g., see Fig. 6 of Steinmetz). Steinmetz still would not involve any providing of a command to a volatile memory cache circuit through a point-to-point channel between an interface circuit and a volatile memory cache circuit as recited in claim 1.

In the Office Action's Response to Arguments section (see paragraph 4 on page 4), the Office Action contends that the language of the independent claim sets forth that a command is provided to a cache through a point-to-point interface, and that the language does not set forth that the cache is directly coupled to the interface over a point-to-point channel. Applicant respectfully submits that such independent claim language is unnecessary since, as explained above, Steinmetz does not disclose providing a command to a volatile memory cache circuit through a point-to-point channel between an interface circuit and a volatile memory cache circuit as recited in claim 1.

For the reasons stated above, claim 1 patentably distinguishes over the cited prior art, and the rejection of claim 1 under 35 U.S.C. §102(e) should be withdrawn. Accordingly, claim 1 is in allowable condition.

Because claims 2-10 and 32-35 depend from and further limit claim 1, claims 2-10 and 32-35 patentably distinguish over the cited prior art for at least the same reasons.

Claims 11-20 and 36-38

Claim 11 is directed to a method for exchanging data with an interface circuit. The method is performed in a volatile memory cache circuit of a data storage system. The method includes the steps of receiving a command from the interface circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit, moving a data element through the point-to-point channel in accordance with the command, and providing status to the

interface circuit through the point-to-point channel in accordance with the data element.

The cited prior art does not teach a method for exchanging data with an interface circuit which has a step of receiving a command from the interface circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit, as recited in claim 11. Rather, as mentioned above in connection with claim 1, Steinmetz discloses an FC controller 206 which communicates with a cache memory 210 through a multi-drop PCI bus 208 (e.g., see column 8, lines 49-52; column 9, lines 1-4 and Fig. 6 of Steinmetz).

If one were to attempt to argue that the FC controller 206 of Steinmetz is an interface circuit, Steinmetz clearly would not involve receiving a command from the interface circuit through a point-to-point channel between the interface circuit and the volatile memory cache circuit as recited in claim 1. Rather, Steinmetz would involve receiving a command through the multi-drop PCI bus 208 through which the microprocessor 212 also communicates (e.g., see Fig. 6 of Steinmetz).

Furthermore, if one were to attempt to argue that the host system 202 is an interface circuit, Steinmetz clearly does not involve providing a command to a volatile memory cache circuit through a point-to-point channel between the interface circuit and a volatile memory cache circuit as recited in claim 1. Rather, Steinmetz would involve receiving a command to an FC controller 206 through an FC between a host system 202 and the FC controller 206 (e.g., see Fig. 6 of Steinmetz). Steinmetz still would not involve any providing of a command to a volatile memory cache circuit through a point-to-point channel between an interface circuit and a volatile memory cache circuit as recited in claim 1.

For the reasons stated above and for similar reasons provided in connection with claim 1, claim 11 patentably distinguishes over the cited prior art, and the rejection of claim 11 under 35 U.S.C. §102(e) should be withdrawn. Accordingly, claim 11 is in allowable condition.

Because claims 12-20 and 36-38 depend from and further limit claim 11, claims 12-20 and 36-38 patentably distinguish over the cited prior art for at least the same reasons.

Claims 21-29 and 39-40

Claim 21 is directed to a data storage system which includes a volatile memory cache circuit that buffers data elements exchanged between a storage device and a host, and an interface circuit that operates as an interface between the volatile memory cache circuit and at least one of the storage device and the host. The data storage system further includes a point-to-point channel interconnected between the volatile memory cache circuit to the interface circuit. The point-to-point channel carries the data elements between the volatile memory cache circuit and the interface circuit.

The cited prior art does not teach a data storage system having a point-to-point channel interconnected between a volatile memory cache circuit to an interface circuit, as recited in claim 21. To the contrary, as explained above in connection with claims 1 and 11, Steinmetz discloses an FC controller 206 which communicates with a cache memory 210 through a multi-drop PCI bus 208. Accordingly, claim 21 patentably distinguishes over the cited prior art for at least the same reasons, and the rejection of claim 21 under 35 U.S.C. §102(e) should be withdrawn. Thus, claim 21 is in allowable condition.

Because claims 22-29 and 39-40 depend from and further limit claim 21, claims 22-29 and 39-40 patentably distinguish over the cited prior art for at least the same reasons.

Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Amendment, that the Application is not in condition for

allowance, the Examiner is respectfully requested to call the Applicant's Representative at the number below.

Applicant hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this Amendment, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-0901.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 366-9600, in Westborough, Massachusetts.

Respectfully submitted,

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